

INSTRUCTION SETS FOR PROCESSORS

[ABSTRACT OF THE DISCLOSURE]

5 A processor has respective first and second
external instruction formats (F_1 , F_2) in which
instructions (add, load) are received by the processor.
Each instruction has an opcode (e.g. 1011) which
specifies an operation to be executed. Each external
format has one or more preselected opcode bits (F_1 :
10 $i+1-i+4$; F_2 : $i+1-i+3$) in which the opcode appears. The
processor also has an internal instruction format (G_1)
into which instructions in the external formats are
translated prior to execution of the operation.

15 A first operation (add) is specifiable in both the
first and second external formats (F_1 , F_2), and a second
operation (load) is specifiable in the second external
format (F_2). The first and second operations have
distinct opcodes (101, 011) in the second external
format. In each of the preselected opcode bits which
20 the first and second external formats have in common
($i+1-i+3$), the opcodes of the first operation (101) in
the two external formats are identical.

25 Such "congruent" instruction encodings can enable
a translation process, for translating the external-
format opcode into a corresponding internal-format
opcode, to be carried out simply and quickly without
the need to positively identify each individual
external-format opcode.

30 [Fig. 3 (B)]